Docket No. 303.098US4
*WD* # 408120

Micron Ref. No. 95-0651.03

**Clean Version of Pending Claims**

LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS
Applicant: Yong-Jun Hu
Serial No.: 09/826,661

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*Claims 31-37 and 39-70, as of January 24, 2002 (date of response to first office action filed).*

31.(Amended) A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second, insulating material;

a generally planar layer of a third, conductive material covering only the bottom surface, the third material including at least two different constituent elements.

32. The contact hole of claim 31 where the third material is an alloy or a composite.

33. The contact hole of claim 32 where the third material contains a refractory metal.

34. The contact hole of claim 32 where the third material is a silicide.

35. The contact hole of claim 32 where the third material is rich in titanium.

36. The contact hole of claim 32 where the stoichiometry of the third material is uniform.

37. The contact hole of claim 31 where the first material is silicon.

39.(Amended) A contact hole for a semiconductor device, comprising:

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a bottom surface of a first material;

at least one vertical sidewall of a second, insulating material and having a high aspect ratio;

a generally planar layer of a third material covering only the bottom surface, the third material including at least two different constituent elements.

40. The contact hole of claim 39 where a height of the sidewall is at least four times a width of the bottom surface.

41. The contact hole of claim 39 where a width of the bottom surface is equal to or less than about 0.5 micron.

42. The contact hole of claim 39 where the third material is substantially confined to the bottom surface of the hole

43.(Amended) A contact hole for a semiconductor device, comprising:

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a bottom surface of a first material;

at least one vertical sidewall of a second material;

a layer of a third material covering only the bottom surface with a thickness variation of less than 50%, the third material including at least two different constituent elements.

44. The contact hole of claim 43 where the thickness variation of the layer is less than about 20%.

45. The contact hole of claim 44 where the thickness variation of the layer is less than about 10%.

46. The contact hole of claim 43 where the planar layer contacts the sidewalls.

47. The contact hole of claim 46 where the planar layer does not extend a substantial distance up the sidewall from the bottom.

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48.(Amended) A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a generally planar layer of a third material covering only the bottom surface, the third material having a graded stoichiometry between two different elements.

49. The contact hole of claim 48 where the hole has a high aspect ratio.

50. The contact hole of claim 48 where the first material is silicon.

51. The contact hole of claim 48 where the second material is an insulator.

52. The contact hole of claim 48 where the planar layer contacts the sidewalls.

53. The contact hole of claim 52 where the third material is substantially confined to the bottom of the hole.

54. The contact hole of claim 48 where the third material is a silicide.

55.(Amended) A contact hole for a semiconductor device, comprising:

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a bottom surface of a first material;

at least one sidewall of an insulating material;

a generally planar layer of a third material covering only the bottom surface, the third material including at least two different constituent elements, none of the third material being present in the sidewall.

56. The contact hole of claim 55 where the insulator is an oxide, a nitride, or a glass.

57. The contact hole of claim 55 where the layer of the third material does not extend substantially up the sidewall from the bottom.

58. The contact hole of claim 55 where the third material is a silicide.

59.(Amended) An integrated circuit, comprising:

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a substrate of a first material;

an insulator of a second material overlying the substrate;

a contact hole through the insulator to the substrate, the contact hole having at least one sidewall of the second material and a generally planar conductive layer located only in a region contacting the substrate, the layer including at least two different constituent elements.

60. The integrated circuit of claim 59 where the substrate is silicon.

61. The integrated circuit of claim 59 where the second material is an oxide, a nitride, or a glass.

62. The integrated circuit of claim 59 where the planar layer contacts the sidewalls.

63.(Amended) The integrated circuit of claim 59 where the layer is planar within a thickness variation less than 50%.

B7 64.(Amended) The integrated circuit of claim 63 where the layer is planar within a thickness variation of about 20%.

65.(Amended) An integrated circuit, comprising:

a substrate of a first material;

an insulator of a second material overlying the substrate;

a multiple contact hole through the insulator to the substrate, the contact hole having at least one sidewall of the second material and a separate generally planar layer of a silicide contacting only the substrate.

66. The integrated circuit of claim 65 where the silicide includes a refractory metal.

67. The integrated circuit of claim 66 where the refractory metal is titanium or cobalt.

68. The integrated circuit of claim 65 where the silicide has a uniform stoichiometry.

69. The integrated circuit of claim 65 where the silicide has at least two different stoichiometries.

70. The integrated circuit of claim 65 where the insulator has a top surface free of the silicide.